ANNA UNIVERSITY, CHENNAI

AFFILIATED INSTITUTIONS

R - 2009

CURRICULUM I SEMESTER (FULL TIME)

M.E. EMBEDDED SYSTEM TECHNOLOGIES

SEMESTER I

SL. No	COURSE CODE	COURSE TITLE	L	T	P	C
THEORY						
1	**MA9216**	Applied Mathematics for Electrical Engineers	3	1	0	4
2	ET9211	Advanced Digital System Design	3	0	0	3
3	ET9212	Micro Controller Based System Design	3	0	0	3
4	ET9213	Design of Embedded Systems	3	0	0	3
5	ET9214	Real Time Systems	3	0	0	3
6		Elective I	3	0	0	3
		TOTAL	**18**	**1**	**0**	**19**

ELECTIVES FOR M.E EMBEDDED SYSTEM TECHNOLOGIES

SEMESTER I

SL. NO	COURSE CODE	COURSE TITLE	L	T	P	C
1	ET9251	Software Technology for Embedded Systems	3	0	0	3
2	PE9275	Soft Computing Techniques	3	0	0	3
3	**AP9222**	Computer Architecture and parallel processing	3	0	0	3

MA 9216 APPLIED MATHEMATICS FOR ELECTRICAL ENGINEERS L T P C
3 1 0 4

UNIT I ADVANCED MATRIX THEORY 12

Eigen-values using QR transformations – Generalized eigen vectors – Canonical forms – Singular value decomposition and applications – Pseudo inverse – Least square approximations.

UNIT II LINEAR PROGRAMMING 12

Formulation – Graphical Solution – Simplex Method – Two Phase Method – Transportation and Assignment Problems.

UNIT III ONE DIMENSIONAL RANDOM VARIABLES 12

Random variables - Probability function – moments – moment generating functions and their properties – Binomial, Poisson, Geometric, Uniform, Exponential, Gamma and Normal distributions – Function of a Random Variable.

UNIT IV QUEUEING MODELS 12

Poisson Process – Markovian queues – Single and Multi Serve r Models – Little's formula – Machine Interference Model – Steady State analysis – Self Service queue.

UNIT V COMPUTATIONAL METHODS IN ENGINEERING 12

Boundary value problems for ODE – Finite difference methods – Numerical solution of PDE – Solution of Laplace and Poisson equations – Liebmann's iteration process – Solution of heat conduction equation by Schmidt explicit formula and Crank-Nicolson implicit scheme – Solution of wave equation.

L +T: 45+15 = 60 PERIODS

REFERENCES

1. Bronson, R., Matrix Operation, Schaum's outline series, McGraw Hill, New York, (1989).
2. Taha, H. A., Operations Research: An Introduction, Seventh Edition, Pearson Education Edition, Asia, New Delhi (2002).
3. R. E. Walpole, R. H. Myers, S. L. Myers, and K. Ye, Probability and Statistics for Engineers & Scientists, Asia, 8th Edition, (2007).
4. Donald Gross and Carl M. Harris, Fundamentals of Queueing theory, 2nd edition, John Wiley and Sons, New York (1985).
5. Grewal, B.S., Numerical methods in Engineering and Science, 7th edition, Khanna Publishers, 200

ET 9211 ADVANCED DIGITAL SYSTEM DESIGN L T P C
3 0 0 3

AIM

To expose the students to the fundamentals of digital logic based system design.

OBJECTIVES

To impart knowledge on

- Basics on Synchronous & Async digital switching design.
- Design & realisation of error free functional blocks for digital systems

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modelling of CSSN – State Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits – ASM Chart – ASM Realization, Design of Arithmetic circuits for Fast adder- Array Multiplier.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA – Test Generation – Masking Cycle – DFT Schemes – Built-in Self Test.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES 9

Programming Techniques -Re-Programmable Devices Architecture- Function blocks, I/O blocks, Interconnects, Realize combinational, Arithmetic, Sequential Circuit with Programmable Array Logic; Architecture and application of Field Programmable Logic Sequence.

UNIT V NEW GENERATION PROGRAMMABLE LOGIC DEVICES 9

Foldback Architecture with GAL, EPLD, EPLA , PEEL, PML; PROM – Realization State machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 - Xilinx 3000

TOTAL: 45 PERIODS

REFERENCES

1. Donald G. Givone, "Digital principles and Design", Tata McGraw Hill 2002.
2. Stephen Brown and Zvonk Vranesic, "Fundamentals of Digital Logic with VHDL Deisgn", Tata McGraw Hill, 2002
3. Mark Zwolinski, "Digital System Design with VHDL", Pearson Education, 2004
4. Parag K Lala, "Digital System design using PLD", BS Publications, 2003
5. John M Yarbrough, "Digital Logic applications and Design", Thomson Learning, 2001
6. Nripendra N Biswas, "Logic Design Theory", Prentice Hall of India, 2001
7. Charles H. Roth Jr., "Fundamentals of Logic design", Thomson Learning, 2004.

ET 9212 MICROCONTROLLER BASED SYSTEM DESIGN L T P C
3 0 0 3

AIM

To expose the students to the fundamentals of microcontroller based system design.

OBJECTIVES

To impart knowledge on

- 8051 Microcontroller based system design.
- Microchip PIC 8 bit microcontroller based system Design

UNIT I 8051 ARCHITECTURE 9

Architecture – memory organization – addressing modes – instruction set – Timers - Interrupts - I/O ports, Interfacing I/O Devices – Serial Communication.

UNIT II 8051 PROGRAMMING 9

Assembly language programming – Arithmetic Instructions – Logical Instructions –Single bit Instructions – Timer Counter Programming – Serial Communication Programming Interrupt Programming – RTOS for 8051 – RTOSLite – FullRTOS –Task creation and run – LCD digital clock/thermometer using FullRTOS

UNIT III PIC MICROCONTROLLER 9

Architecture – memory organization – addressing modes – instruction set – PIC progrmming in Assembly & C –I/O port, Data Conversion, RAM & ROM Allocation, Timer programming, MP-LAB.

UNIT IV PERIPHERAL OF PIC MICROCONTROLLER 9

Timers – Interrupts, I/O ports- I^2C bus-A/D converter-UART- CCP modules -ADC, DAC and Sensor Interfacing –Flash and EEPROM memories.

UNIT V SYSTEM DESIGN – CASE STUDY 9

Interfacing LCD Display – Keypad Interfacing - Generation of Gate signals for converters and Inverters - Motor Control – Controlling AC appliances –Measurement of frequency - Stand alone Data Acquisition System.

TOTAL: 45 PERIODS

REFERENCES

1. Muhammad Ali Mazidi, Rolin D. Mckinlay, Danny Causey ‘ PIC Microcontroller and Embedded Systems using Assembly and C for PIC18’, Pearson Education 2008
2. John Iovine, ‘PIC Microcontroller Project Book ’, McGraw Hill 2000
3. Myke Predko, “Programming and customizing the 8051 microcontroller”, Tata McGraw Hill 2001.

ET 9213 DESIGN OF EMBEDDED SYSTEMS L T P C
3 0 0 3

UNIT I EMBEDDED DESIGN LIFE CYCLE 9

Product specification – Hardware / Software partitioning – Detailed hardware and software design – Integration – Product testing – Selection Processes – Microprocessor Vs Micro Controller – Performance tools – Bench marking – RTOS Micro Controller – Performance tools – Bench marking – RTOS availability – Tool chain availability – Other issues in selection processes.

UNIT II PARTITIONING DECISION 9

Hardware / Software duality – coding Hardware – ASIC revolution – Managing the Risk – Co-verification – execution environment – memory organization – System startup – Hardware manipulation – memory mapped access – speed and code density.

UNIT III INTERRUPT SERVICE ROUTINES 9

Watch dog timers – Flash Memory basic toolset – Host based debugging – Remote debugging – ROM emulators – Logic analyser – Caches – Computer optimisation – Statistical profiling

UNIT IV IN CIRCUIT EMULATORS 9

Buller proof run control – Real time trace – Hardware break points – Overlay memory – Timing constraints – Usage issues – Triggers.

UNIT V TESTING 9

Bug tracking – reduction of risks & costs – Performance – Unit testing – Regression testing – Choosing test cases – Functional tests – Coverage tests – Testing embedded software – Performance testing – Maintenance.

TOTAL : 45 PERIODS

REFERENCES

1. Arnold S. Berger – “Embedded System Design”, CMP books, USA 2002.
2. Sriram Iyer, “Embedded Real time System Programming”
3. ARKIN, R.C., Behaviour-based Robotics, The MIT Press, 1998.

ET 9214 REAL TIME SYSTEMS L T P C
3 0 0 3

UNIT I INTRODUCTION 9

Introduction – Issues in Real Time Computing – Structure of a Real Time System – Task classes – Performance Measures for Real Time Systems – Estimating Program Run Times – Task Assignment and Scheduling – Classical uniprocessor scheduling algorithms – Uniprocessor scheduling of IRIS tasks – Task assignment – Mode changes and Fault Tolerant Scheduling.

UNIT II PROGRAMMING LANGUAGES AND TOOLS 9

Programming Languages and Tools – Desired language characteristics – Data typing – Control structures – Facilitating Hierarchical Decomposition, Packages, Run time (Exception) Error handling – Overloading and Generics – Multitasking – Low level programming – Task Scheduling – Timing Specifications – Programming Environments – Run – time support**.**

UNIT III REAL TIME DATABASES 9

Real time Databases – Basic Definition, Real time Vs General Purpose Databases, Main Memory Databases, Transaction priorities, Transaction Aborts, Concurrency control issues, Disk Scheduling Algorithms, Two – phase Approach to improve Predictability – Maintaining Serialization Consistency – Databases for Hard Real Time Systems.

UNIT IV COMMUNICATION 9

Real – Time Communication – Communications media, Network Topologies Protocols, Fault Tolerant Routing. Fault Tolerance Techniques – Fault Types – Fault Detection. Fault Error containment Redundancy – Data Diversity – Reversal Checks – Integrated Failure handling.

UNIT V EVALUATION TECHNIQUES 9

Reliability Evaluation Techniques – Obtaining parameter values, Reliability models for Hardware Redundancy – Software error models. Clock Synchronization – Clock, A Nonfault – Tolerant Synchronization Algorithm – Impact of faults – Fault Tolerant Synchronization in Hardware – Fault Tolerant Synchronization in software.

TOTAL : 45 PERIODS

TEXT BOOKS

1. C.M. Krishna, Kang G. Shin, “Real – Time Systems”, McGraw – Hill International Editions, 1997.
2. Rajib Mall, ”Real-time systems: theory and practice”, Pearson Education, 2007
3. Peter D.Lawrence, “Real Time Micro Computer System Design – An Introduction”, McGraw Hill, 1988.
4. Stuart Bennett, “Real Time Computer Control – An Introduction”, Prentice Hall of India, 1998.
5. S.T. Allworth and R.N.Zobel, “Introduction to real time software design”, Macmillan, 2nd Edition, 1987.
6. R.J.A Buhur, D.L Bailey, “An Introduction to Real – Time Systems”, Prentice – Hall International, 1999.
7. Philip.A.Laplante, “Real Time System Design and Analysis”, Prentice Hall of India, 3rd Edition, April 2004.

ET 9251 SOFTWARE TECHNOLOGY FOR EMBEDDED SYSTEMS L T P C
3 0 0 3

UNIT I PROGRAMMING EMBEDDED SYSTEMS 9

Embedded Program – Role of Infinite loop – Compiling, Linking and locating – downloading and debugging – Emulators and simulators processor – External peripherals – Toper of memory – Memory testing – Flash Memory.

UNIT II C AND ASSEMBLY 9

Overview of Embedded C - Compilers and Optimization - Programming and Assembly – Register usage conventions – typical use of addressing options – instruction sequencing – procedure call and return – parameter passing – retrieving parameters – everything in pass by value – temporary variables

UNIT III. EMBEDDED PROGRAM AND SOFTWARE DEVELOPMENT PROCESS 9

Program Elements – Queues – Stack- List and ordered lists-Embedded programming in C++ - Inline Functions and Inline Assembly - Portability Issues - Embedded Java- Software Development process: Analysis – Design- Implementation – Testing – Validation- Debugging - Software maintenance

UNIT IV UNIFIED MODELLING LANGUAGE 9

Object State Behaviour – UML State charts – Role of Scenarios in the Definition of Behaviour – Timing Diagrams – Sequence Diagrams – Event Hierarchies – Types and Strategies of Operations – Architectural Design in UML Concurrency Design – Representing Tasks – System Task Diagram – Concurrent State Diagrams – Threads. Mechanistic Design – Simple Patterns

UNIT V WEB ARCHITECTURAL FRAMEWORK FOR EMBEDDED SYSTEM 9

Basics – Client/sever model- Domain Names and IP address – Internet Infrastructure and Routing – URL – TCP/IP protocols - Embedded as Web Client - Embedded Web servers - HTML - Web security - Case study : Web-based Home Automation system.

TOTAL : 45 PERIODS

REFERENCES:

1. David E.Simon: “An Embedded Software Primer”, Pearson Education, 2003
2. Michael Barr, “Programming Embedded Systems in C and C++”, Oreilly, 2003
3. H.M. Deitel , P.J.Deitel, A.B. Golldberg “ Internet and World Wide Web – How to Program” Third Edition , Pearson Education , 2001.
4. Bruce Powel Douglas, “Real-Time UML, Second Edition: Developing Efficient Object for Embedded Systems, 2nd edition ,1999, Addison-Wesley
5. Daniel W.lewis “Fundamentals of Embedded Software where C and Assembly meet” PHI 2002.
6. Raj Kamal, “Embedded Systems- Architecture, Programming and Design” Tata McGraw Hill, 2006.

PE9275 SOFT COMPUTING TECHNIQUES L T P C
3 0 0 3

UNIT I INTRODUCTION 9

Approaches to intelligent control. Architecture for intelligent control. Symbolic reasoning system, rule-based systems, the AI approach. Knowledge representation. Expert systems.

UNIT II ARTIFICIAL NEURAL NETWORKS 9

Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron. Learning and Training the neural network. Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations. Hopfield network, Self-organizing network and Recurrent network. Neural Network based controller

UNIT III FUZZY LOGIC SYSTEM 9

Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning. Introduction to fuzzy logic modeling and control. Fuzzification, inferencing and defuzzification. Fuzzy knowledge and rule bases. Fuzzy modeling and control schemes for nonlinear systems. Self-organizing fuzzy logic control. Fuzzy logic control for nonlinear time-delay system.

UNIT IV GENETIC ALGORITHM 9

Basic concept of Genetic algorithm and detail algorithmic steps, adjustment of free parameters. Solution of typical control problems using genetic algorithm. Concept on some other search techniques like tabu search and anD-colony search techniques for solving optimization problems.

UNIT V APPLICATIONS 9

GA application to power system optimisation problem, Case studies: Identification and control of linear and nonlinear dynamic systems using Matlab-Neural Network toolbox.
Stability analysis of Neural-Network interconnection systems. Implementation of fuzzy logic controller using Matlab fuzzy-logic toolbox. Stability analysis of fuzzy control systems.

TOTAL : 45 PERIODS

REFERENCES

1. Jacek.M.Zurada, "Introduction to Artificial Neural Systems", Jaico Publishing House, 1999.
2. KOSKO,B. "Neural Networks And Fuzzy Systems", Prentice-Hall of India Pvt. Ltd., 1994.
3. KLIR G.J. & FOLGER T.A. "Fuzzy sets, uncertainty and Information", Prentice-Hall of India Pvt. Ltd., 1993.
4. Zimmerman H.J. "Fuzzy set theory-and its Applications"-Kluwer Academic Publishers, 1994.
5. Driankov, Hellendroon, "Introduction to Fuzzy Control", Narosa Publishers.

AP 9222	COMPUTER ARCHITECTURE AND PARALLEL PROCESSING	L T P C 3 0 0 3

UNIT I THEORY OF PARALLELISM 9

Parallel Computer models – the state of computing, Multiprocessors and Multicomputers and Multivectors and SIMD computers, PRAM and VLSI models, Architectural development tracks, Program and network properties – Conditions of parallelism.

UNIT II PARTITIONING AND SCHEDULING 9

Program partitioning and scheduling, Program flow mechanisms, System interconnect architectures, Principles of scalable performance – performance matrices and measures, Parallel processing applications, speedup performance laws, scalability analysis and approaches.

UNIT III HARDWARE TECHNOLGIES 9

Processor and memory hierarchy advanced processor technology, superscalar and vector processors, memory hierarchy technology, virtual memory technology, bus cache and shared memory – backplane bus systems, cache memory organizations, shared memory organizations, sequential and weak consistency models.

UNIT IV PIPELINING AND SUPERSCALAR TECHNOLOGIES 9

Parallel and scalable architectures, Multiprocessor and Multicomputers, Multivector and SIMD computers, Scalable, Multithreaded and data flow architectures.

UNIT V SOFTWARE AND PARALLEL PROCESSING 9

Parallel models, Languages and compilers, Parallel program development and environments, UNIX, MACH and OSF/1 for parallel computers.

TOTAL : 45 PERIODS

REFERENCES:

1. Kai Hwang “Advanced Computer Architecture”. McGraw Hill International 2001.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, “Advanced computer Architecture – A design Space Approach”. Pearson Education,2003.
3. Carl Homacher, Zvonko Vranesic, Sefwat Zaky, “Computer Organisation”, 5th Edition, TMH, 2002.
4. David E. Culler, Jaswinder Pal Singh with Anoop Gupta “Parallel Computer Architecture” ,Elsevier, 2004.
5. John P. Shen. “Modern processor design Fundamentals of super scalar processors”, Tata McGraw Hill 2003.
6. Sajjan G. Shiva “Advanced Computer Architecture”, Taylor & Francis, 2008.
7. V.Rajaraman, C.Siva Ram Murthy, “Parallel Computers- Architecture and Programming”, Prentice Hall India, 2008.
8. John L. Hennessy, David A. Petterson, “Computer Architecture: A Quantitative Approach”, 4th Edition, Elsevier, 2007.
9. Harry F. Jordan Gita Alaghaband, “Fundamentals of Parallel Processing”. Pearson Education, 2003.
10. Richard Y. Kain, “Advanced computer architecture – A system Design Approach”, PHI, 2003.